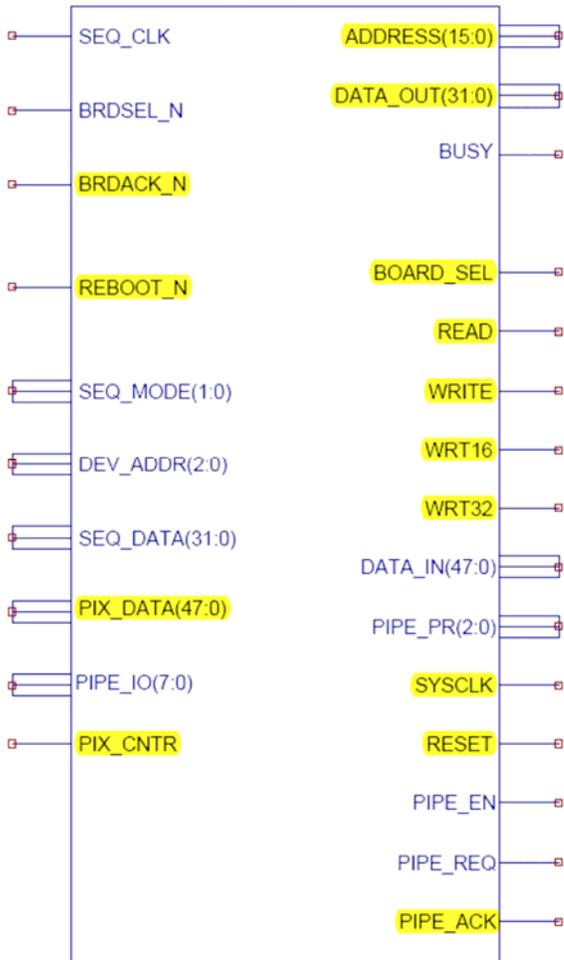


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```
-----  
-- DESCRIPTION :  
-- IMPLEMENTS A STANDARD INTERFACE BETWEEN THE MONSOON BUS SYSTEM AND  
-- ANY PERIPHERAL BOARD.  
-----  
-- IMPLEMENTATION NOTES :  
-- THIS IMPLEMENTATION CONFORMS TO MONSOON ICD 7.9  
-- DOCUMENT NUMBER MNSN-xx-XX-xx  
-- IT GENERALLY IS APPLICABLE TO ALL NOAO MONSOON PERIPHERAL BOARDS UNDER  
-- REVISION '0'.  
--  
-- NOTE: THIS VERSION SPECIFICALLY FOR IR ACQUISITION BOARD USES ONLY A 16 BIT  
-- DATA OUT PATH.  
--  
-- THIS MODULE CONTAINS THE FOLLOWING SUB ASSEMBLIES:  
-- CLOCK : USED AND PASSED STRAIGHT THROUGH  
-- BOARD SELECT : ENABLES THE MODE DECODE LOGIC  
-- MODE : DECODES THE SEQUENCER MODE AND ASSERTS THE CORRECT SIGNALS  
-- RESET : SYNCHRONOUSLY DECODED TO PROVIDE SOFT RESET AND HARD REBOOT SIGNALS  
-- ADDRESS MUX : SELECTS THE CORRECT ADDRESS DEPENDING ON WHETHER 32 OR 16 BIT MODE  
-- ASSERTED  
-- SEQ BUS DATA MUX : DEMULTIPLEXES THE DATA FROM THE BUS.  
-- PIXEL BUS TRISTATES : ENABLES THE PIXEL DATA BUS TO TRANSMIT DATA TO THE MCB  
-- PIPELINE REQUEST LOGIC : HANDLES THE ACCESS TO THE PIXEL DATA BUS DURING PIPELINE WRITES.  
--  
-- THE VISION IS THAT USING THIS TEMPLATE AS A STARTING POINT, ANY FUTURE  
-- PERIPHERAL BOARD WILL BE ABLE TO PERSONALIZE THIS MODULE TO SUIT THEIR  
-- PARTICULAR REQUIREMENTS. TO USE THIS TEMPLATE, IMPORT IT INTO YOUR DESIGN  
-- AS A LOCAL PROJECT FILE AND HACK AWAY TO MAKE IT WORK FOR YOU.  
-----
```

## seq\_ifc\_7091



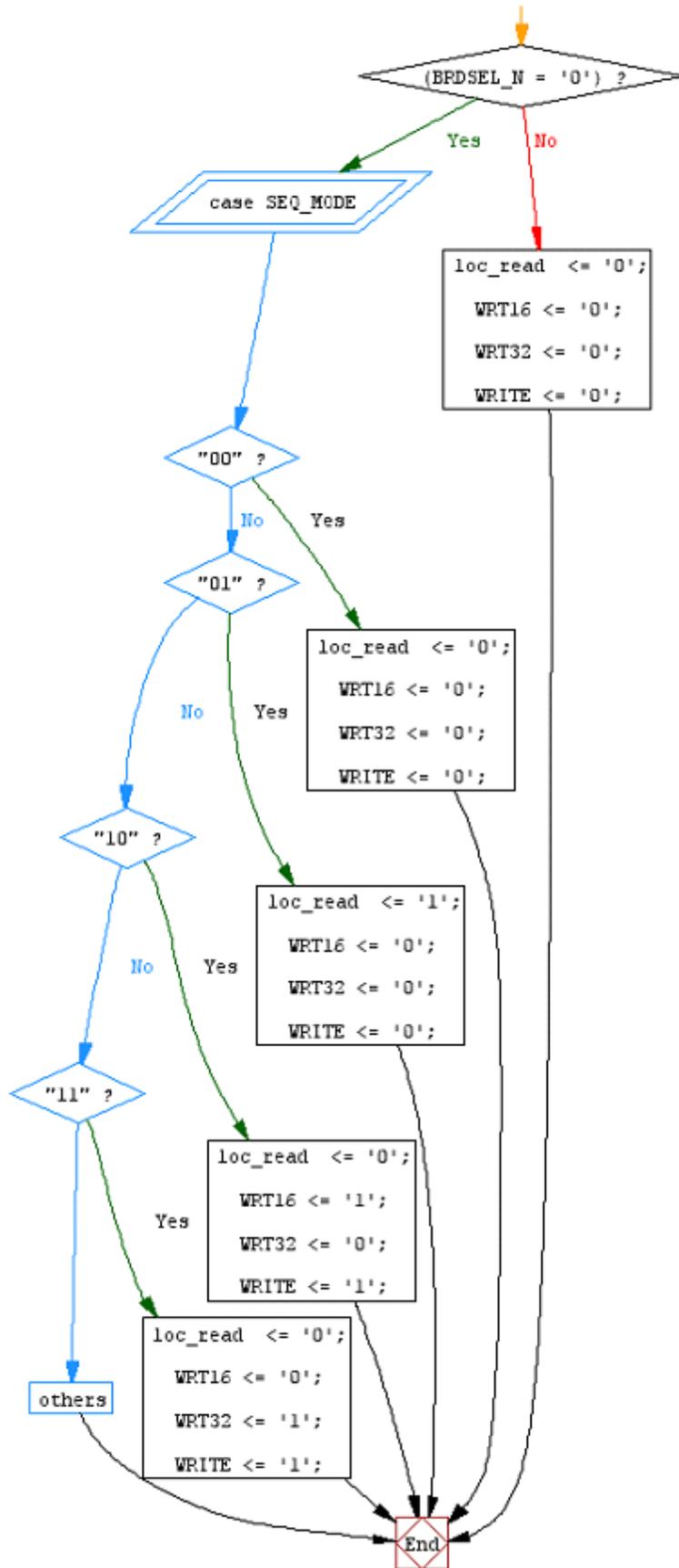
4/5/2006

```
SYSCLK      : in  std_logic;  
RST_CMD     : in  std_logic;  
SYNC_RCVD   : in  std_logic;  
ASYNC_FLAG  : out std_logic;  
RESET_OUT   : out std_logic
```

```
--      constant BootRstPer : std_logic_vector(19 downto 0) := x"92C70";  
--      Period of boot reset pulse (15 ms = 92C70h).  
constant BootRstPer : std_logic_vector(19 downto 0) := x"00005";  
--      Period of boot reset pulse (15 ms = 927C0h).  test only.  
constant ExtRstPer  : std_logic_vector(19 downto 0) := x"00028";  
--      Period of normal reset pulse (1 us = 28h).  
constant ExtRstPer  : std_logic_vector(19 downto 0) := x"00008";  
--      Period of normal reset pulse (1 us = 28h)      test only.  
signal RstPeriod    : std_logic_vector(19 downto 0);  
signal RstCounter   : std_logic_vector(19 downto 0);  
signal BootFlag     : std_logic := '0';  
signal LocalRst     : std_logic;
```

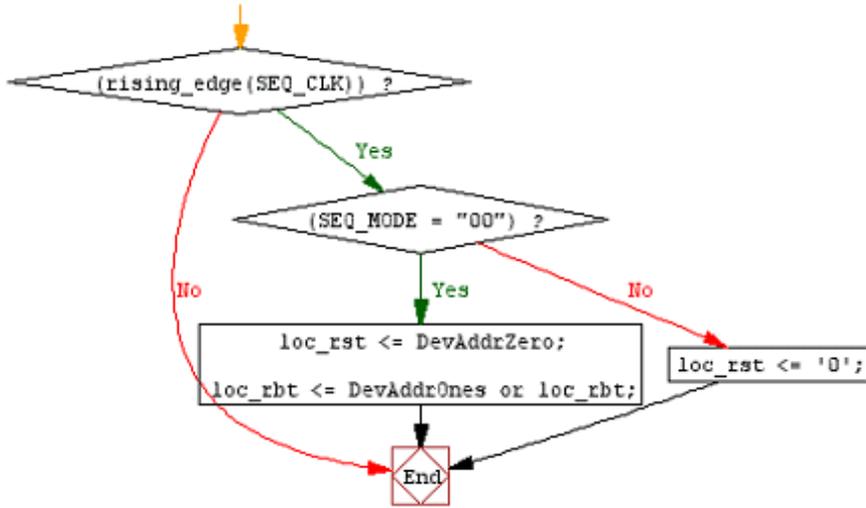
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ModeDecode : process (SEQ\_MODE, BRDSEL\_N)



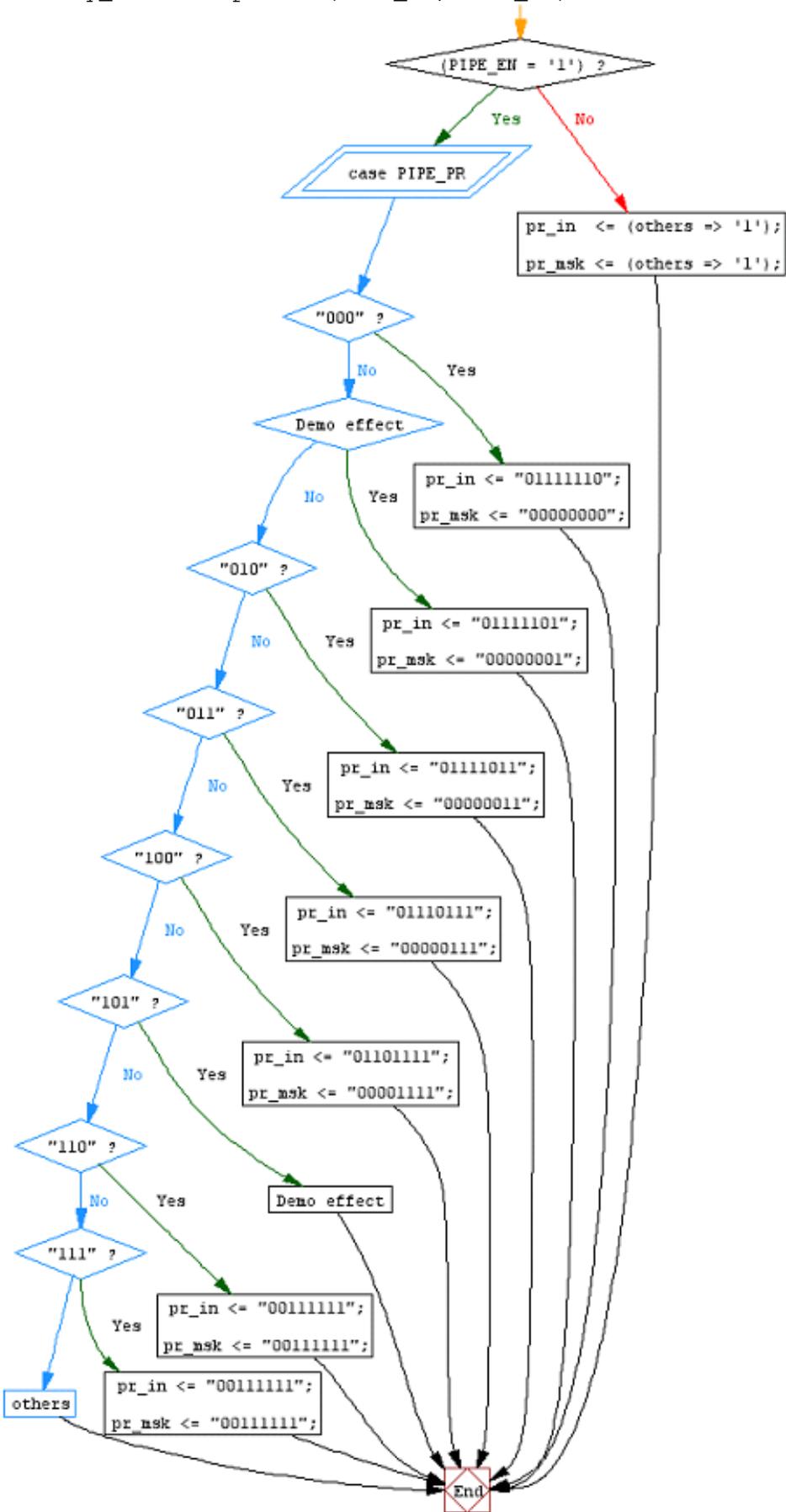
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ResetState : process(SEQ\_CLK)



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priority\_decode : process(PIPE\_PR, PIPE\_EN)



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PipeWriteFsm : process (SEQ\_CLK, loc\_rst, PIPE\_EN)

